

SIMPLE GENERATION OF NEGATIVE BIAS VOLTAGE FOR POWER DRIVER APPLICATIONS

By Vincent Dessard, X-REL Semiconductor

TABLE OF CONTENTS

Introduction	2
First Proposed Architecture	2
Simulation Results (First Architecture)	4
Second Proposed Architecture	5
Simulation results (2 nd architecture).....	5
Conclusions	6
Important Notice & Disclaimer	7
Contact Us	7

ABSTRACT

This Application Note describes an original implementation to generate the negative bias voltage to drive power transistors, while using a power driver supplied with only a positive voltage. The particularity of the proposed implementation is that only few low-cost devices are added, not requiring any external negative power supply.

INTRODUCTION

In order to correctly turn on and off some switches, such as SiC transistors, it is usually required to drive its gate between a positive and a negative supply voltage (+20V and -5V for SiC MOSFETs, for example). Often, the control signal is a 0/5V logic signal with respect to the ground level. Then, to provide the driving levels including a negative voltage, it is required to use a power driver that performs the level shifting operation between the positive and negative supplies, as well as a negative supply voltage. This can degrade the global efficiency in some DCDC applications, in particular if the negative supply has to also bias the driver as it would represent easily few mA of DC current.

This application note presents two original implementations of a power driver generating on its own the negative drive level with an efficient method. It is based on a single XTR25010 driver together with an external high-temperature diode (e.g. XTR1N0415) and an external high-temperature zener device.

FIRST PROPOSED ARCHITECTURE

The simplified schematic of the first architecture proposed is presented in Figure 1. The main idea of this architecture is to shift the common mode of the drive signal with 20V span (in this example) by an amount determined by the voltage on zener diode D_{Z1} .

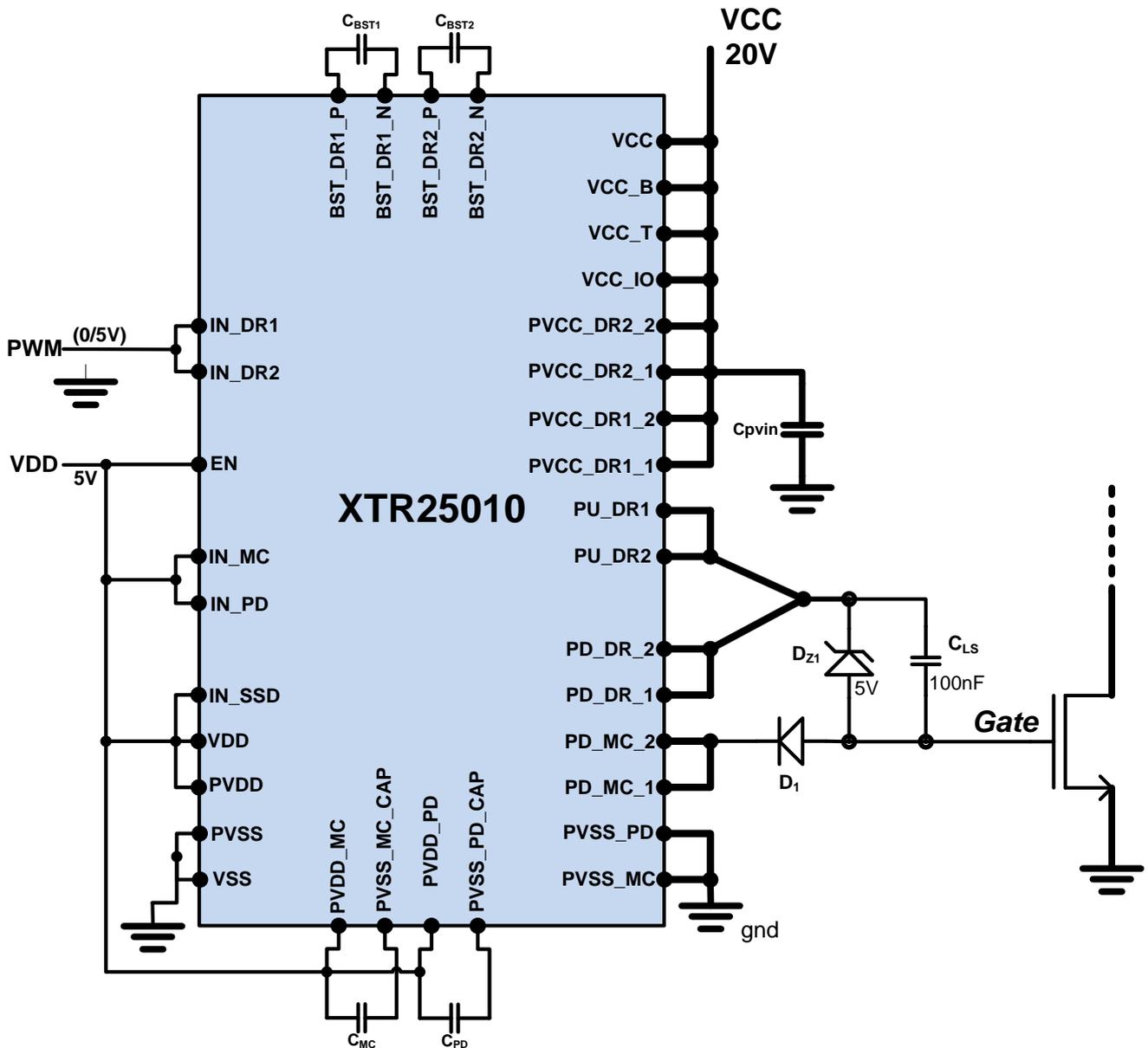


Figure 1. Implementation of the first architecture.

An equivalent simplified functional view of the previous figure is sketched in Figure 2.

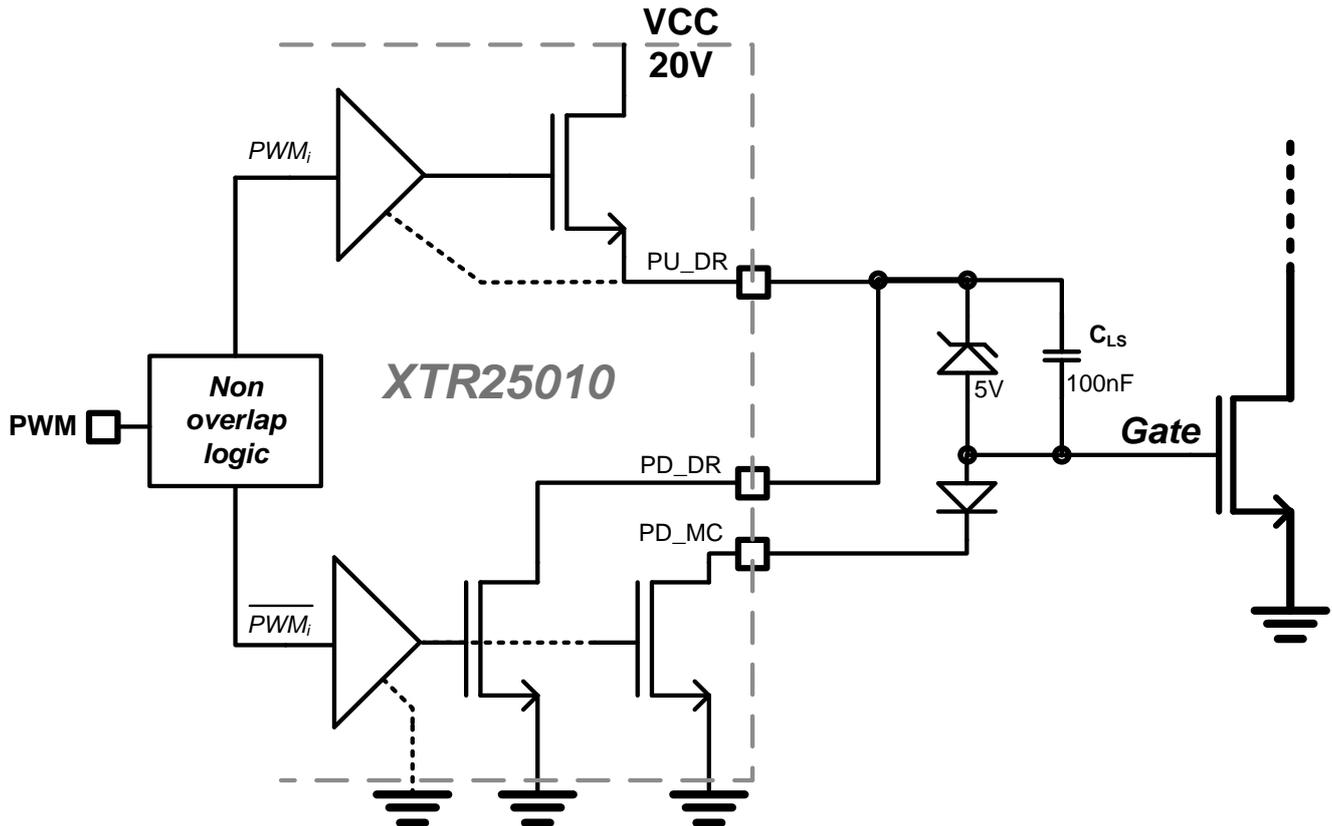


Figure 2. Functional block diagram of the output stage of the self biasing driver.

At the very beginning it is supposed that the external capacitor C_{LS} is discharged. Assume that this capacitor is much larger than the gate capacitance of the output power switch. This means that the first PWM pulses would appear on the gate of the power transistor with drive levels between V_{CC} (20V) and GND (0V). Progressively, at each turn on of the PWM signal, the pull-up current responsible for charging C_{gs} would flow across C_{LS} , charging this latter too. On the other side, at each turn off of the PWM, the C_{gs} capacitor will mostly be discharged across the pull-down "PD_MC" access, without significantly discharging C_{LS} . There is therefore an effect of charge pumping on C_{LS} as it is more charged than discharged at each PWM cycle, until a steady state is reached. After few PWM cycles, the C_{LS} capacitor voltage drop will reach its steady state value corresponding to the nominal voltage of zener D_{Z1} . From that moment on, C_{LS} capacitor can be considered as a simple DC level shifter. As the common node PU_DR (connected to PD_DR) is switching between V_{CC} and zero, it means that the Gate node will switch between $V_{CC}-V_{DZ1}$ and $-V_{DZ1}$.

Thanks to this intrinsic charge pump effect, the XTR25010 does not need to be supplied by a negative supply voltage, resulting in increased power efficiency. Also, the XTR25010 lower level being at ground, its PWM input can directly be connected to a standard PWM signal (referred to gnd) without any need of level shifting.

SIMULATION RESULTS (FIRST ARCHITECTURE)

Figure 3 shows simulation results of the output stage of the XTR25010 using the configuration described in the previous section. The upper green wave is the applied 200kHz PWM input signal. On the lower part of the image, the yellow wave represents the VCC supply (20V) and the blue wave is the output V_{gs} . For this simulation a 1nF capacitor load was used instead of the power MOSFET. We can see that the first blue pulse is reaching VCC (20V). However, after few tens of pulses, the output level is shifted down by about 5V (i.e. by the zener voltage).

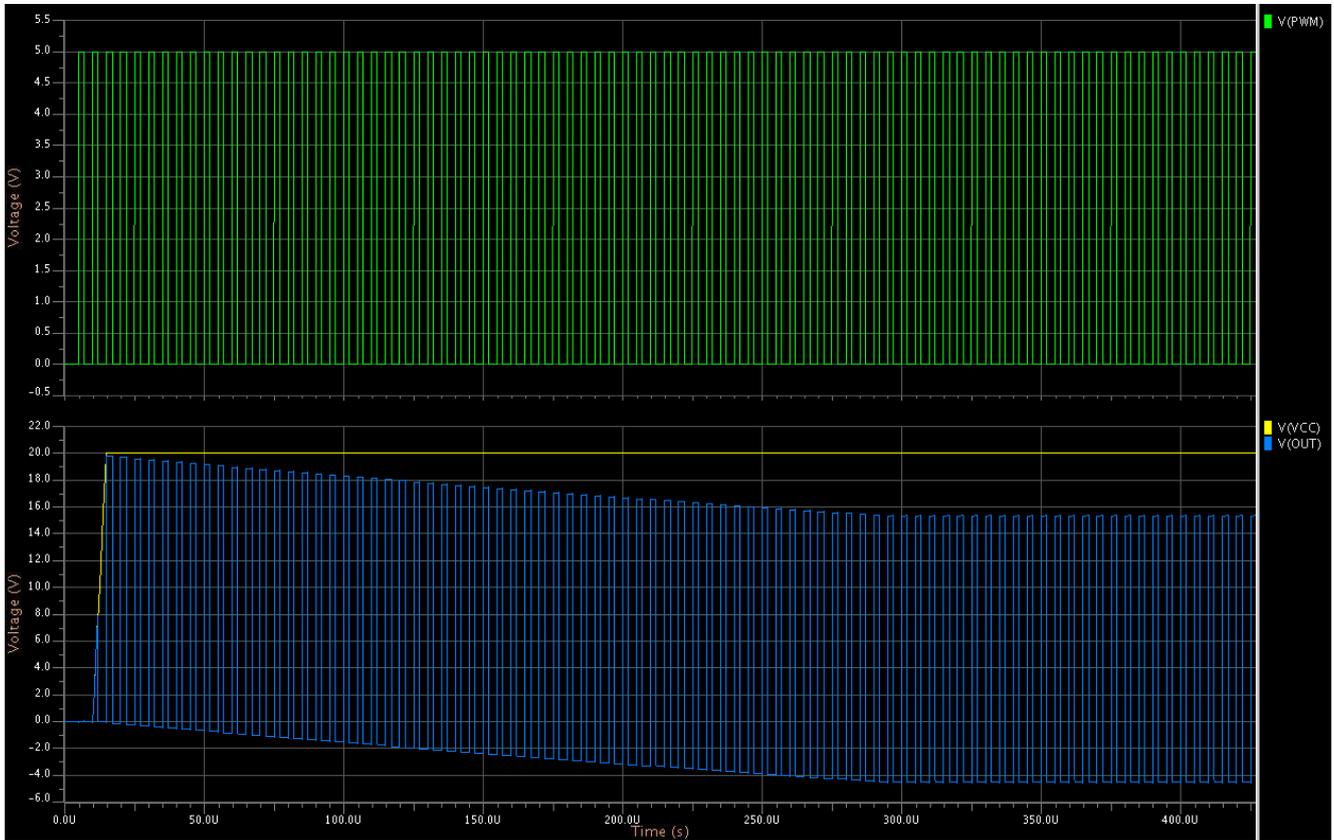


Figure 3. Simulation results of the first architecture.

Note that with this first architecture, with a 20V supply, the first pulse reaches 20V while in steady state, pulses are stabilized between +15V and -5V. For DCDC applications with high voltage operation but limited power level, having 15V instead of 20V on the gate will slightly increase the on-resistance of the switching device. Nevertheless, at moderate power levels, this increase of the on-resistance would not be critical. Note that if $V_{CC}=25V$ is used, stable drive levels would be -5V and +20V, as expected. However, the first pulses would be at +25V, which could damage the switching device.

In case it is really critical to reach the upper V_{gs} drive level without any initial over voltage, the first proposed architecture can be slightly improved as sketched in the next section.

SECOND PROPOSED ARCHITECTURE

Compared to the previous architecture, a second zener diode (D_{z2}) of 20V is added as well as a diode D_2 . In order to avoid over currents, the addition of the nominal voltages of both zener diodes must be at least equal to the VCC supply voltage. With this last proposal, the initial pulse will be at about 21V ($V_{z2} + V_{FWD_D2}$). Then, in steady state, once C_{LS} is charged at its 5V nominal value, the V_{gs} voltage will switch between -5V and +20V as expected.

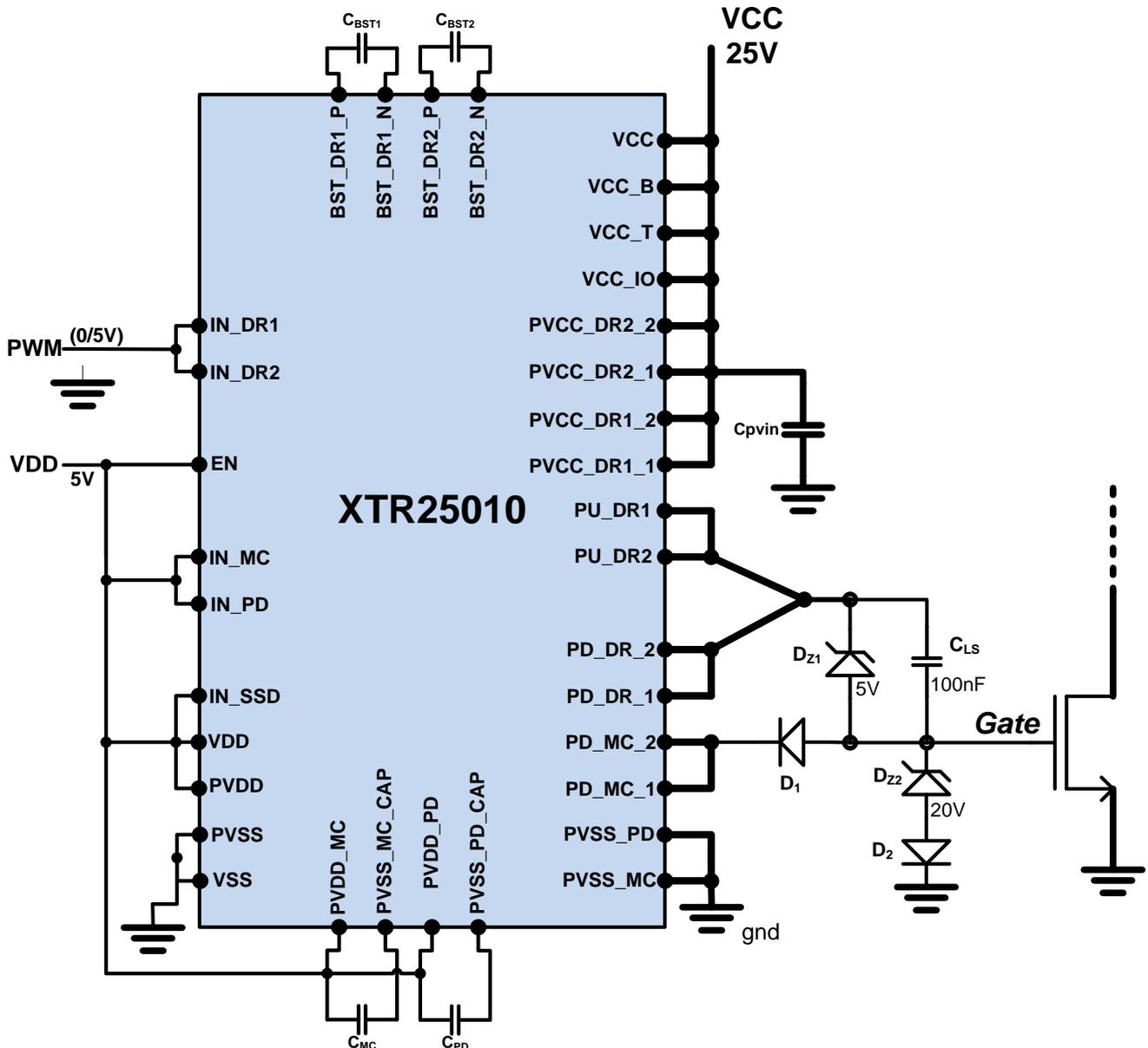


Figure 4. Implementation of the second architecture.

SIMULATION RESULTS (2ND ARCHITECTURE)

Here below in Figure 5 are the simulation results of the output stage of the second architecture. The steady state regime appears much earlier than in the first architecture. The initial maximum V_{gs} value is not very aggressive compared to the steady state maximum V_{gs} value. This architecture is therefore better than the first one at the cost of two additional passive elements.

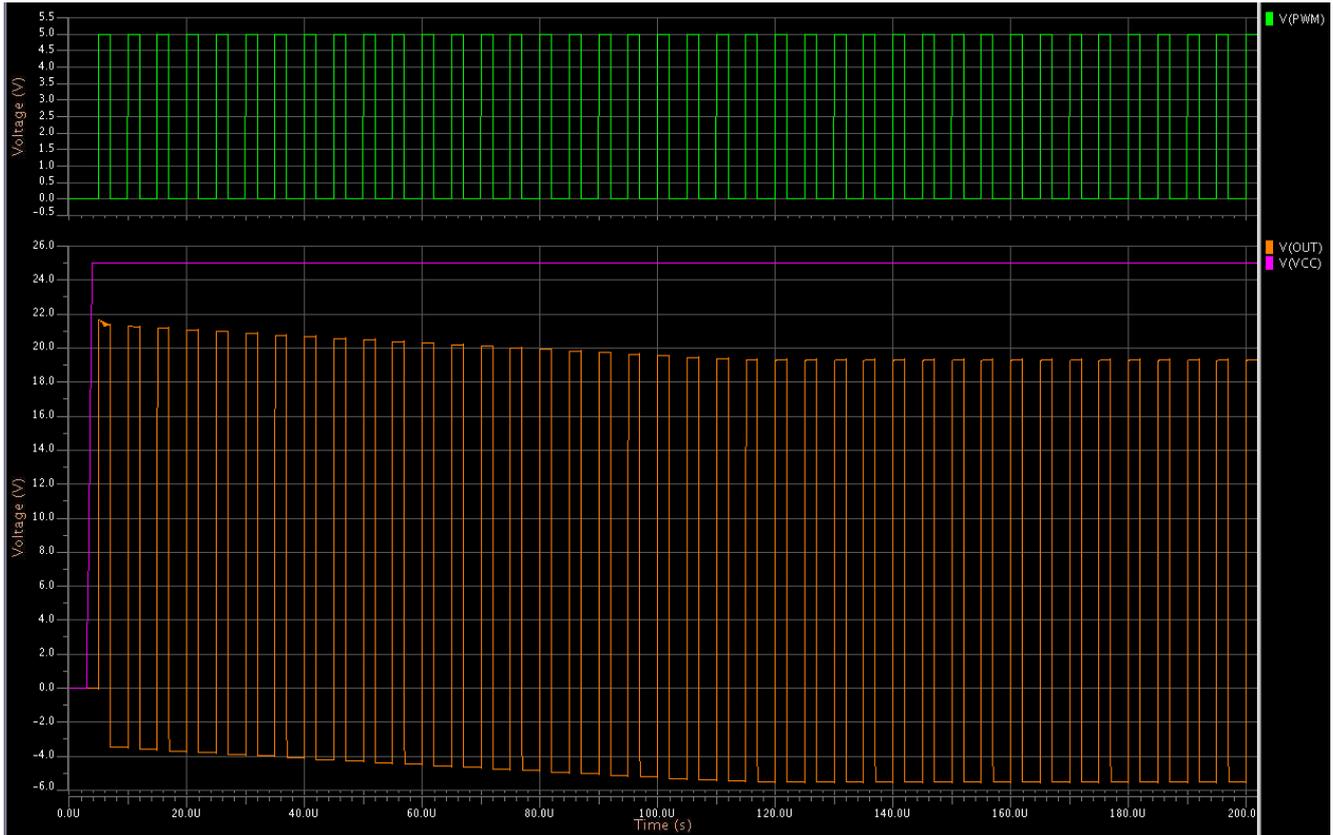


Figure 5. Simulation results of the second architecture.

CONCLUSIONS

Solutions proposed in the Application Note to drive a power device needing a negative turn off voltage with only a positive supply voltage are extremely simple and much less expensive than implementing a complete negative power supply.

Notice that, in both architectures proposed, the precision on the absolute value of used zener devices at high temperature can be quite poor. This needs to be taken into account when sizing the elements and selecting the VCC value. For most low to medium power application, the first (simpler) proposed architecture is probably sufficient.

IMPORTANT NOTICE & DISCLAIMER

Information in this document supersedes and replaces all information previously supplied. Information in this document is provided solely in connection with X-REL Semiconductor products.

The information contained herein is believed to be reliable. X-REL Semiconductor makes no warranties regarding the information contained herein. X-REL Semiconductor assumes no responsibility or liability whatsoever for any of the information contained herein. X-REL Semiconductor assumes no responsibility or liability whatsoever for the use of the information contained herein. The information contained herein is provided "AS IS, WHERE IS" and with all faults, and the entire risk associated with such information is entirely with the user. X-REL Semiconductor reserves the right to make changes, corrections, modifications or improvements, to this document and the information herein without notice. Customers should obtain and verify the latest relevant information before placing orders for X-REL Semiconductor products. The information contained herein or any use of such information does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other intellectual property rights, whether with regard to such information itself or anything described by such information.

Unless expressly approved in writing by an authorized representative of X-REL Semiconductor, X-REL Semiconductor products are not designed, authorized or warranted for use in military, aircraft, space, life saving, or life sustaining applications, nor in products or systems where failure or malfunction may result in personal injury, death, or property or environmental damage.

General Sales Terms & Conditions apply.

CONTACT US

For more information on X-REL Semiconductor's products, technical support or ordering:

- ✓ Web: www.x-relsemi.com/products
- ✓ Tel: +33 456 580 580
- ✓ Fax: +33 456 580 599
- ✓ Sales: sales@x-relsemi.com
www.x-relsemi.com/EN/Sales-Representatives
- ✓ Information: info@x-relsemi.com
- ✓ Support: support@x-relsemi.com

X-REL Semiconductor

90, Avenue Léon Blum
38100 Grenoble
France