HIGH-TEMPERATURE MULTI-FUNCTION LOGIC GATES

FEATURES

- ▲ Operational beyond the -60°C to +230°C temperature range.
- ▲ Supply voltage from 2.8V to 5.5V.
- ▲ Schmitt trigger inputs.
- ▲ Compatible with NAND, NOR, XOR, INVERTER functions of the standard 54HC family.
- ▲ Latch-up free.
- ▲ Ruggedized SMT and thru-hole packages.
- ▲ Also available as bare die.

APPLICATIONS

- ▲ Reliability-critical, Automotive, Aeronautics & Aerospace, Down-hole.
- ▲ Combinatorial logic circuits.

DESCRIPTION

XTR54000 is a configurable logic device able to provide four different functions from the same silicon part. The full featured part is available in a 16-pin package where two pins are used to select the corresponding logic function of the other left-aligned 14 pins. Available functions are 2-input NAND, NOR, XOR, INVERTER.

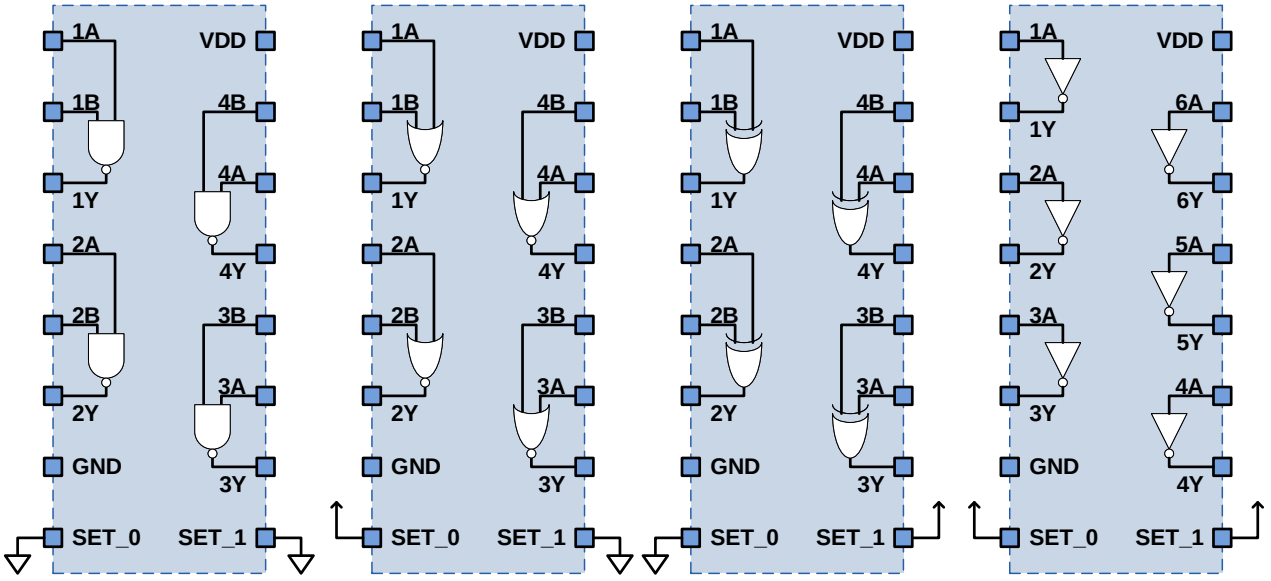
The logic function can also be selected during assembly into 14-pin packages offering pin-to-pin compatibility with standard parts from the 54HC family.

In all configurations, all inputs are Schmitt trigger for increased noise margin.

XTR54000 parts have been designed to reduce system cost and ease adoption by reducing the learning curve and providing smart and easy to use features.

Parts from the XTR54000 family are available in ruggedized SMT and thru-hole packages. Parts are also available as bare dies.

PRODUCT HIGHLIGHT



SET_0=0 / SET_1=0
Quad Schmitt Trigger
2-input NAND

SET_0=1 / SET_1=0
Quad Schmitt Trigger
2-input NOR

SET_0=0 / SET_1=1
Quad Schmitt Trigger
2-input XOR

SET_0=1 / SET_1=1
Hex Schmitt Trigger
INVERTER

ORDERING INFORMATION

X	TR	54	000
Source: X = X-REL Semi	Process: TR = HiTemp, HiRel R = HiRel	Part family	Part number

Product Reference	Description	Temperature Range	Package	Pin Count	Marking
XTR54000-D	Configurable device	-60°C to +230°C	Ceramic side braze DIP	16	XTR54000
XTR54000-S	Configurable device	-60°C to +230°C	Ceramic SOIC	16	XTR54000
XTR54000-TD	Configurable device	-60°C to +230°C	Tested Bare die		

Other packages and packaging configurations possible upon request. For some packages or packaging configurations, MOQ may apply.

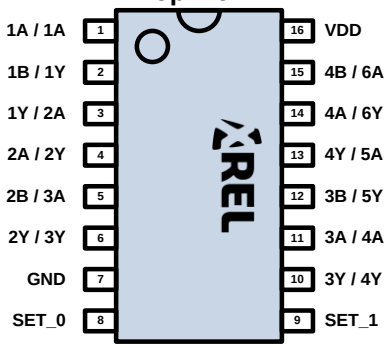
ABSOLUTE MAXIMUM RATINGS

Supply voltage VDD to GND (V_{DD})	-0.5 to 6V
Voltage on any pin, input or output, to GND	-0.5 to V_{DD}+0.5V
Input clamp current I_{IK} (V_I<0 or V_I>V_{DD})	±20mA
Output clamp current I_{OK} (V_O<0 or V_O>V_{DD})	±20mA
Continuous output current I_O (V_O=0 to V_{DD})	±20mA
Storage Temperature Range	-70°C to +230°C
Operating Junction Temperature Range	-70°C to +300°C
ESD Classification	2kV HBM MIL-STD-883

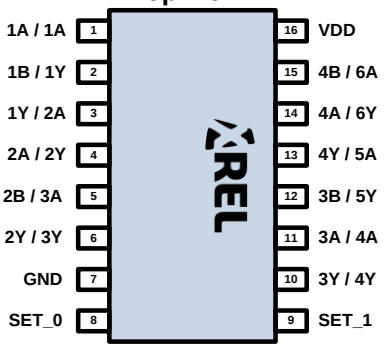
Caution: *Stresses beyond those listed in "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only and functionality of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to "ABSOLUTE MAXIMUM RATINGS" conditions for extended periods may permanently affect device reliability.*

PRODUCT VARIANTS

Side Brazed DIP16
XTR54000-D
Top view



Ceramic SOIC16
XTR54000-S
Top view



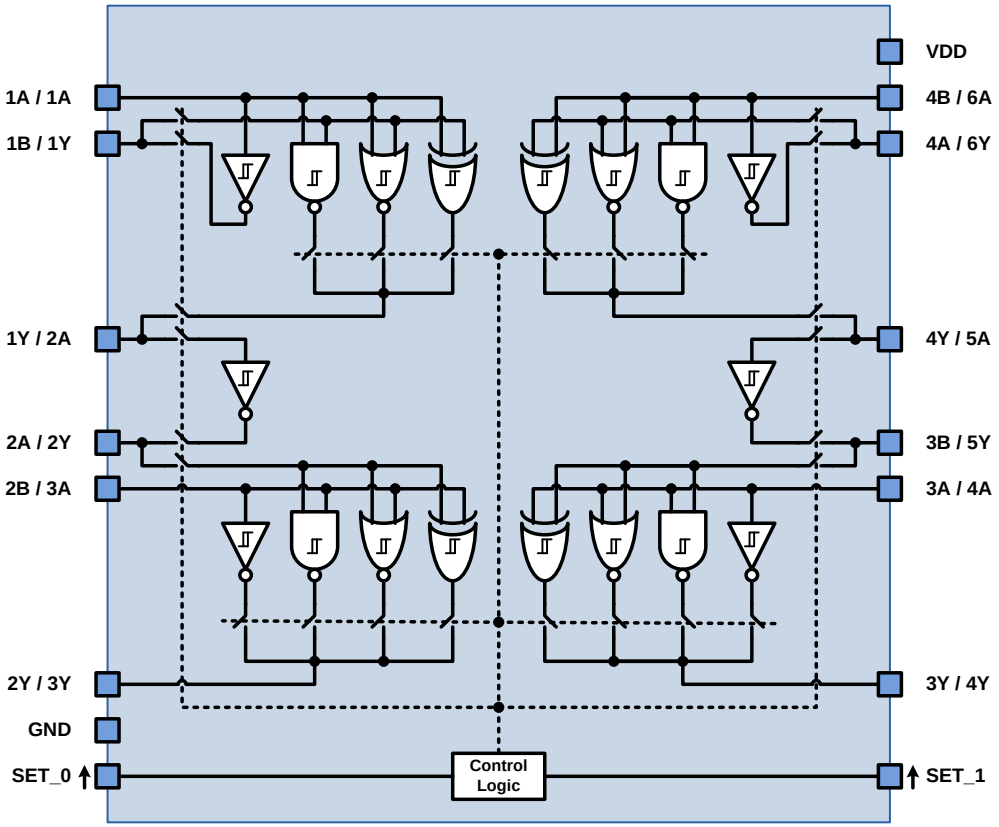
Reconfigurable NAND / NOR / XOR / INV
Schmitt Trigger Inputs

Table 1. Function Selection Table

SET_1	SET_0	Function
0	0	Quad 2-input NAND
0	1	Quad 2-input NOR
1	0	Quad 2-input XOR
1	1	Hex INVERTER[1]

[1] Default configuration when SET_0 and SET_1 are left floating.

BLOCK DIAGRAM



Arrows aside pin names indicate whether the input is internally pulled up.

PIN DESCRIPTION

XTR54000		
Pin Number	**Name**	**Description**
1	**1A / 1A**	Input A of first 2-input gate / Input of first inverter.
2	**1B / 1Y**	Input B of first 2-input gate / Output of first inverter.
3	**1Y / 2A**	Output of first 2-input gate / Input of second inverter.
4	**2A / 2Y**	Input A of second 2-input gate / Output of second inverter.
5	**2B / 3A**	Input B of second 2-input gate / Input of third inverter.
6	**2Y / 3Y**	Output of second 2-input gate / Output of third inverter.
7	**GND**	Circuit ground.
8	**SET_0**	LSB of function selection bits. Internally pulled-up.
9	**SET_1**	MSB of function selection bits. Internally pulled-up.
10	**3Y / 4Y**	Output of third 2-input gate / Output of fourth inverter.
11	**3A / 4A**	Input A of third 2-input gate / Input of fourth inverter.
12	**3B / 5Y**	Input B of third 2-input gate / Output of fifth inverter.
13	**4Y / 5A**	Output of fourth 2-input gate / Input of fifth inverter.
14	**4A / 6Y**	Input A of fourth 2-input gate / Output of sixth inverter.
15	**4B / 6A**	Input B of fourth 2-input gate / Input of sixth inverter.
16	**VDD**	Supply voltage.

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Supply voltage **V_{DD}**	2.8		5.5	V
Voltage on any pin, input or output, with respect to GND.	0		V_{DD}	V
Ambient Temperature[1] **T_{amb}**	-60		230	°C

[1] Operation beyond the specified temperature range is achieved.

ELECTRICAL SPECIFICATIONS

Unless otherwise stated, specification applies for V_{DD}=5V, -60°C<T_{amb}<230°C.

Parameter	Condition	Min	Typ	Max	Units
Supply					
Supply voltage **V_{DD}**		2.8		5.5	V
Supply quiescent current **I_{DD}**	SET_0=SET_1=VDD.T_{amb}=230°C. V_{DD}=2.8V V_{DD}=5.5V		3.5 4.3	10 15	µA
	SET_0=VDD and SET_1=0 or SET_0=0 and SET_1=VDD.T_{amb}=230°C. V_{DD}=2.8V V_{DD}=5.5V		10 18	20 30	µA
	SET_0=SET_1=0.T_{amb}=230°C. V_{DD}=2.8V V_{DD}=5.5V		16 29	35 50	µA
SET_0 and SET_1 pull-up strength (per input) **I_{PU}**	Pulled-up inputs SET_1 or SET_0 forced to GND. T_{amb}=-60°C T_{amb}=230°C		6 12	12 20	µA
Power dissipation capacitance **C_{PD}**[1]	SET_0=SET_1=VDD		8.5	14	pF
	SET_0=VDD & SET_1=0, SET_0=0 & SET_1=VDD or SET_0=SET_1=0.		10	16	
Schmitt Trigger Inputs					
Positive-going input threshold **V_{T+}**	V_{DD}=2.8V V_{DD}=5.5V		2.0 3.4	2.3 3.8	V
Negative-going input threshold **V_{T-}**	V_{DD}=2.8V V_{DD}=5.5V	0.6 1.2	0.9 1.9		V
Hystereris voltage (V_{T+}-V_{T-}) **V_{Hys}**	V_{DD}=2.8V V_{DD}=5.5V	0.5 0.8	1.1 1.5		V
Outputs					
HIGH-level output voltage **V_{OH}**	I_{OUT}=-4mA (device sourcing). T_{amb}=230°C. V_{DD}=2.8V V_{DD}=5.5V	2.35 5.20	2.58 5.38		V
	I_{OUT}=-8mA (device sourcing). T_{amb}=230°C. V_{DD}=3.3V V_{DD}=5.5V	2.7 5.00	2.97 5.25		
LOW Level ouput voltage **V_{OL}**	I_{OUT}=4mA (device sinking). T_{amb}=230°C. V_{DD}=3.3V V_{DD}=5.5V		0.21 0.11	0.35 0.25	V
	I_{OUT}=8mA (device sinking). T_{amb}=230°C. V_{DD}=3.3V V_{DD}=5.5V		0.33 0.22	0.6 0.40	
Timing					
Propagation delay from inputs A or B to output Y **t_{PHL}**	C_L=50pF, T_{amb}=25°C. V_{DD}=2.8V V_{DD}=5.5V		27 13	50 25	ns
	C_L=50pF, T_{amb}=230°C. V_{DD}=2.8V V_{DD}=5.5V		37 18	60 30	
Propagation delay from inputs A or B to output Y **t_{PLH}**	C_L=50pF, T_{amb}=25°C. V_{DD}=2.8V V_{DD}=5.5V		33 11	60 22	ns
	C_L=50pF, T_{amb}=230°C. V_{DD}=2.8V V_{DD}=5.5V		39 14	65 25	
Output transition time. Any output Y. **t_{THL} / t_{TLH}**	C_L=50pF, T_{amb}=25°C. V_{DD}=2.8V V_{DD}=5.5V		7 2	14 5	ns
	C_L=50pF, T_{amb}=230°C. V_{DD}=2.8V V_{DD}=5.5V		8 3	16 7	

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in W):

$P_D = C_{PD} \times V_{DD}^2 \times \sum(f_i) + \sum(C_{Lo} \times V_{DD}^2 \times f_o)$

With:
- V_{DD} = supply voltage in V
- f_i = switching frequency of input “i” (in Hz).
- $\sum(f_i)$ = sum of all input switching frequencies (in Hz).
- C_{Lo} = load capacitance on output “o” (in F)
- f_o = switching frequency of output “o” (in Hz).
- $\sum(C_{Lo} \times V_{DD}^2 \times f_o)$ = sum of all output power dissipations (in W).

XTR54000 TYPICAL PERFORMANCE

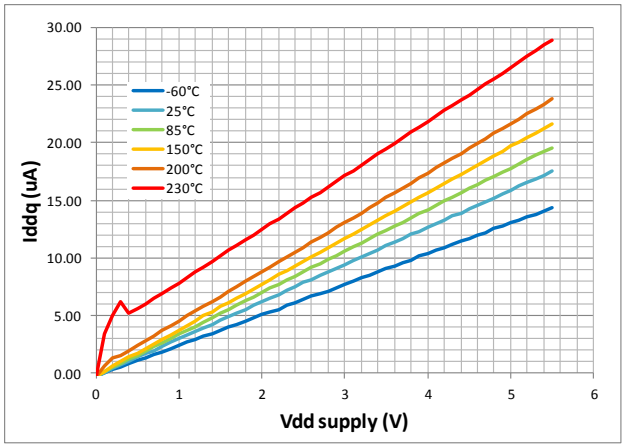


Figure 1. Total Quiescent Current (I_{DD}) vs. Supply Voltage for different Case Temperatures with inputs to GND or VDD. SET_0=0 and SET_1=0 (Quad 2-input NAND configuration)

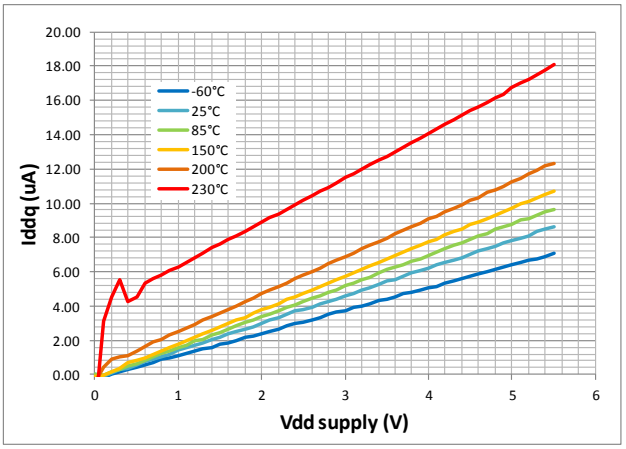


Figure 2. Total Quiescent Current (I_{DD}) vs. Supply Voltage for different Case Temperatures with inputs to GND or VDD. SET_0=0 and SET_1=1 (Quad 2-input NOR configuration)

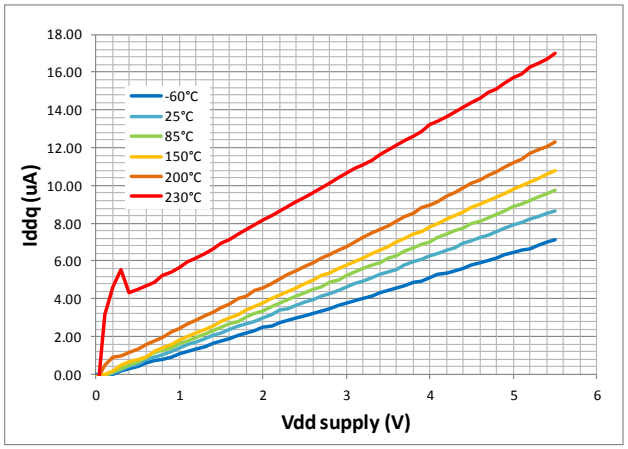


Figure 3. Total Quiescent Current (I_{DD}) vs. Supply Voltage for different Case Temperatures with inputs to GND or VDD. SET_0=1 and SET_1=0 (Quad 2-input XOR configuration)

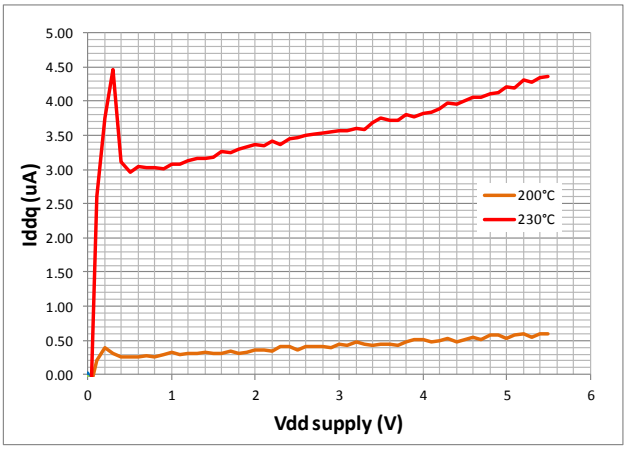


Figure 4. Total Quiescent Current (I_{DD}) vs. Supply Voltage for different Case Temperatures with inputs to GND or VDD. SET_0=1 and SET_1=1 (Hex INVERTER configuration)

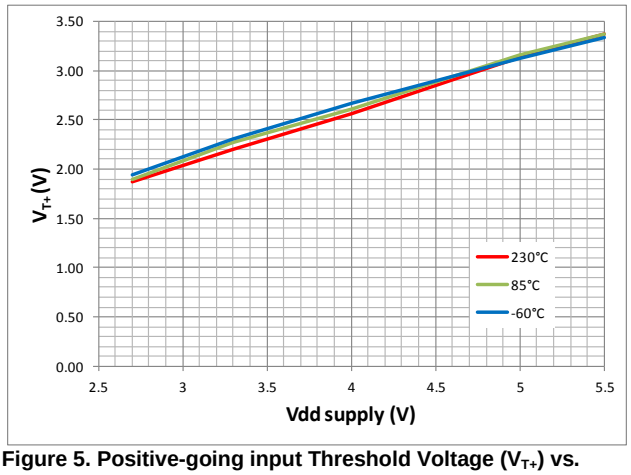


Figure 5. Positive-going input Threshold Voltage (V_{T+}) vs. Supply Voltage for different Case Temperatures.

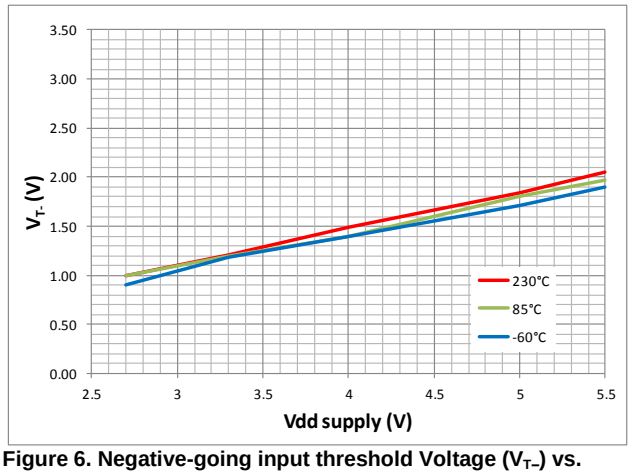


Figure 6. Negative-going input threshold Voltage (V_{T-}) vs. Supply Voltage for different Case Temperatures.

XTR54000 TYPICAL PERFORMANCE (CONTINUED)

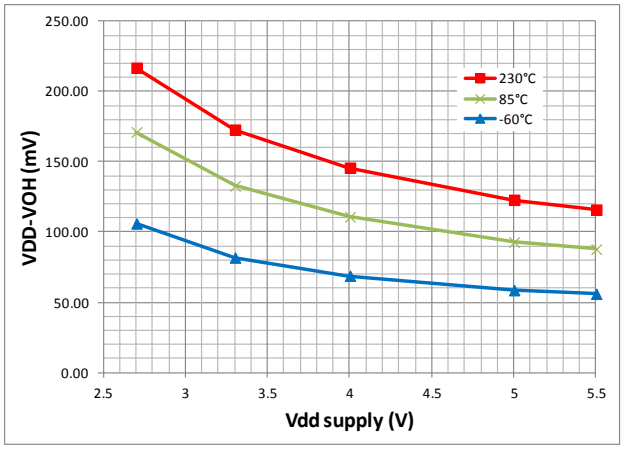


Figure 7. HIGH-level Output Voltage (V_{OH}) vs. Supply Voltage for different Case Temperatures and Iout=4mA sinking.

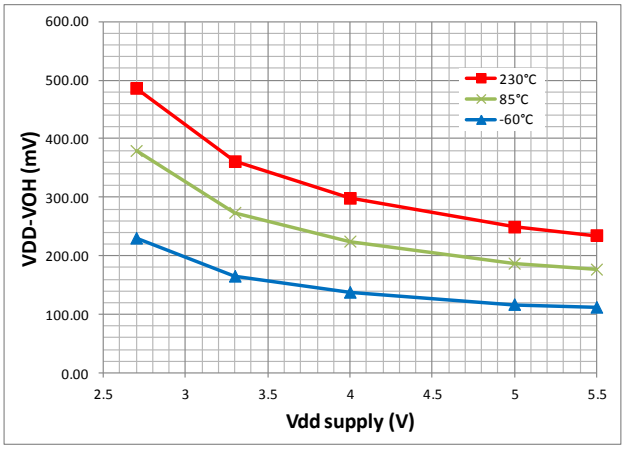


Figure 8. HIGH-level Output Voltage (V_{OH}) vs. Supply Voltage for different Case Temperatures and Iout=8mA sinking.

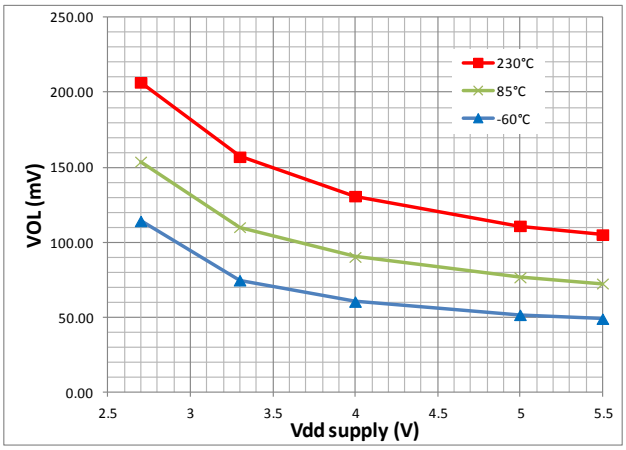


Figure 9. LOW-level Output Voltage (V_{OL}) vs. Supply Voltage for different Case Temperatures and Iout=4mA sourcing.

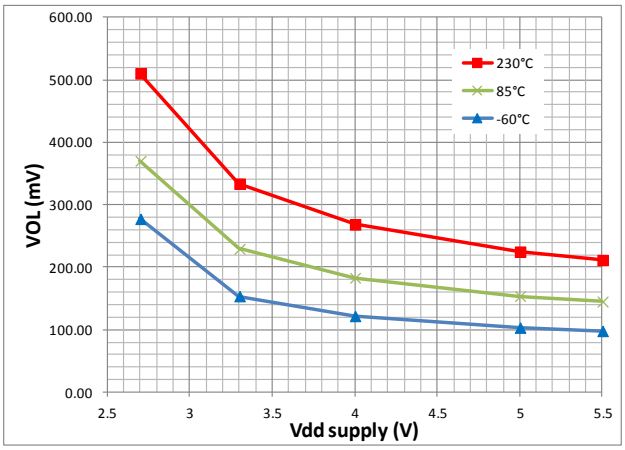


Figure 10. LOW-level Output Voltage (V_{OL}) vs. Supply Voltage for different Case Temperatures and Iout=8mA sourcing.

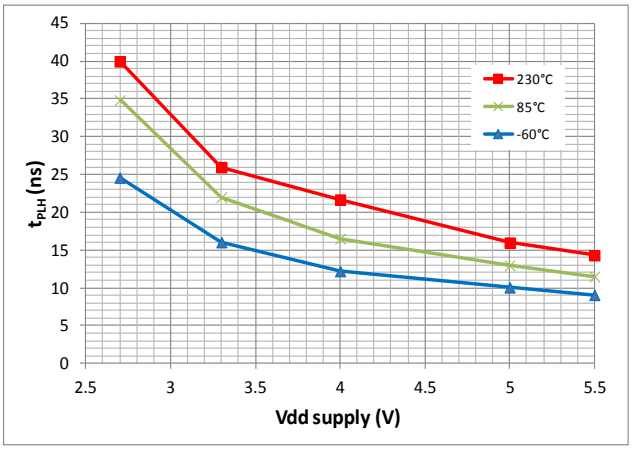


Figure 11. Propagation Delay (t_{PLH}) vs. Case Temperature for different Supply Voltages.
Rising Input to rising Output and C_L =50pF.

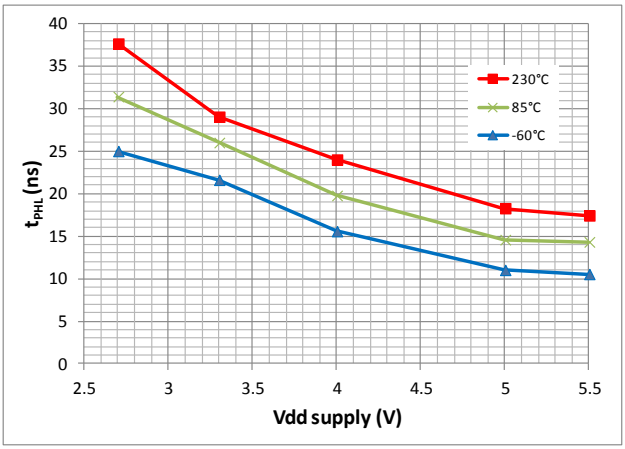


Figure 12. Propagation Delay (t_{PHL}) vs. Case Temperature for different Supply Voltages.
Falling Input to falling Output and C_L =50pF.

XTR54000 TYPICAL PERFORMANCE (CONTINUED)

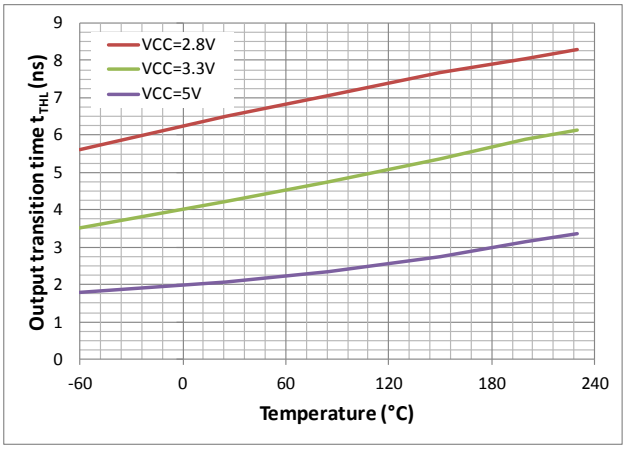


Figure 13. Output transition time (t_{THL}) vs. Case Temperature for different Supply Voltages.
High to Low output and C_L =50pF.

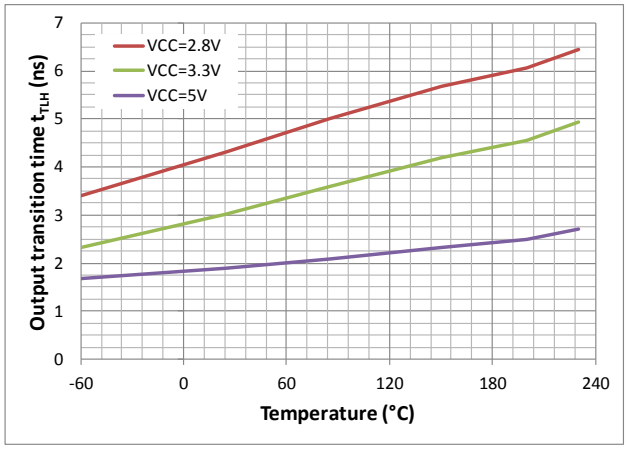
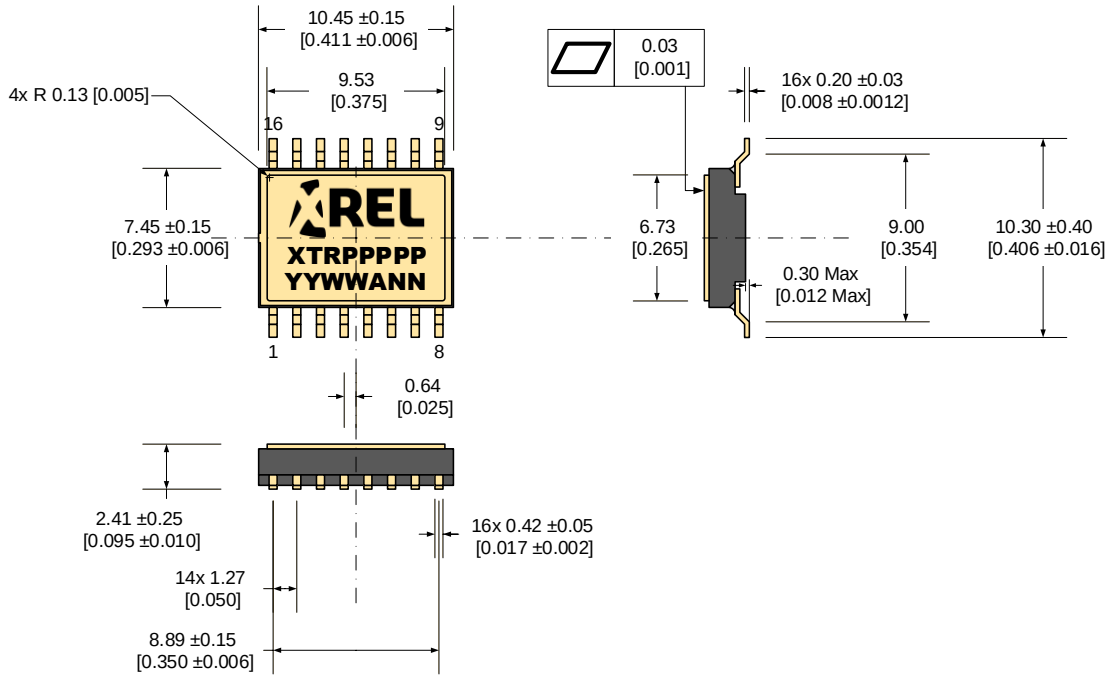


Figure 14. Output transition time (t_{TLL}) vs. Case Temperature for different Supply Voltages.
Low to High output and C_L =50pF.

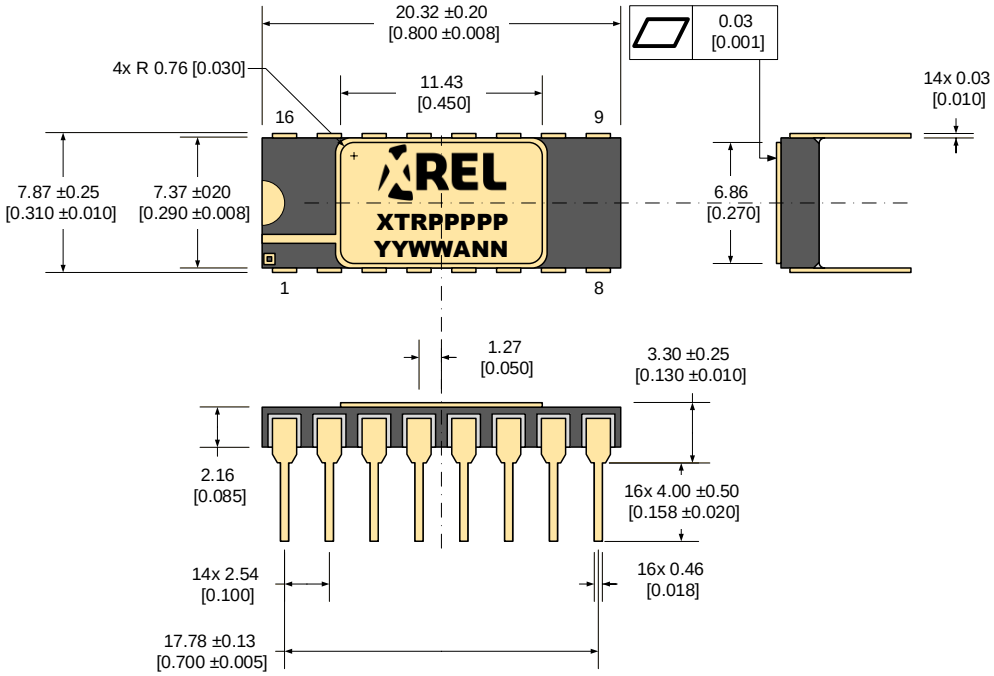
PACKAGE OUTLINES

Dimensions shown in mm [inches]. Tolerances ±0.13 mm [±0.005 in] unless otherwise stated.

Ceramic Small Outline IC SOIC16



Ceramic Side Brazed Dual In-line DIP16



Part Marking Convention	
Part Reference: XTRPPPPPP	
XTR	X-REL Semiconductor, high-temperature, high-reliability product (XTRM Series).
PPPPP	Part number (0-9, A-Z).
Unique Lot Assembly Code: YYWWANN	
YY	Two last digits of assembly year (e.g. 11 = 2011).
WW	Assembly week (01 to 52).
A	Assembly location code.
NN	Assembly lot code (01 to 99).

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